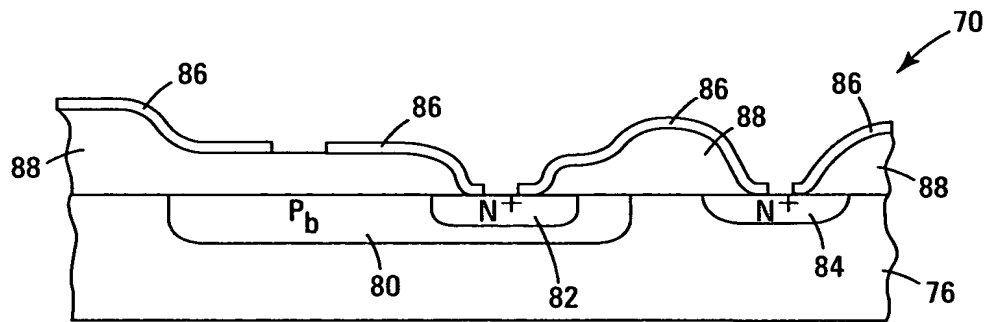
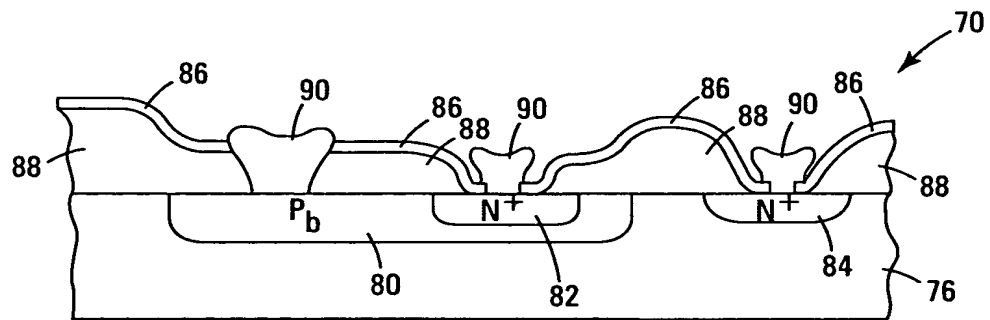


*Fig. 1B*  
*(Prior Art)*



*Fig. 2A*  
(Prior Art)

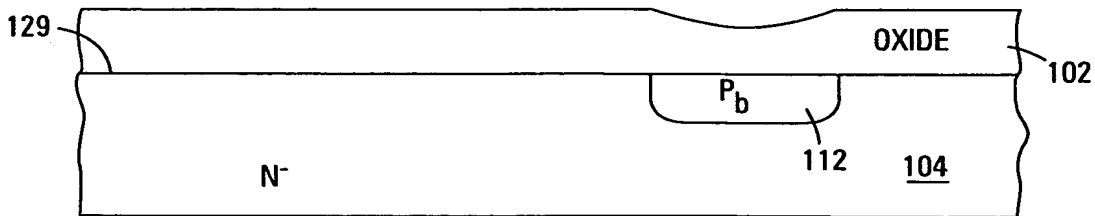


*Fig. 2B*  
(Prior Art)

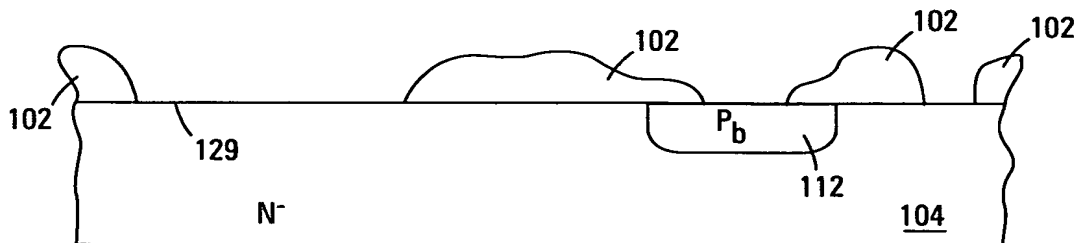
James D. Beasom  
INTEGRATED CIRCUIT WITH MOS CAPACITOR  
Atty Dkt. No. 125.014US01 Serial No. 09/992,880



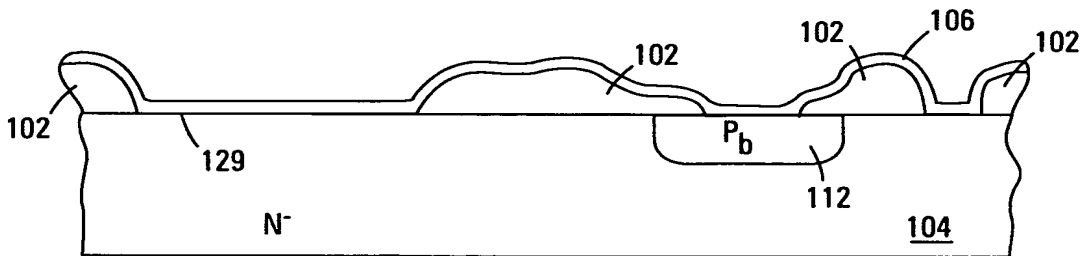
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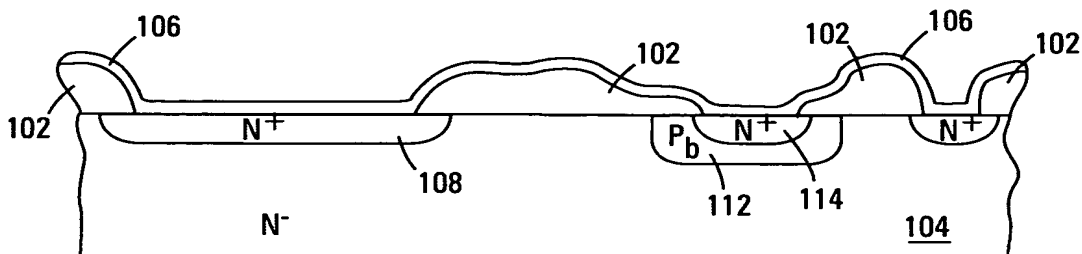
*Fig. 4A*



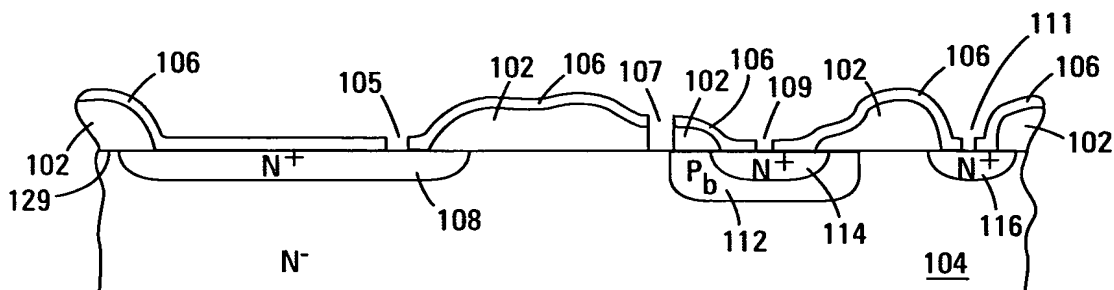
*Fig. 4B*



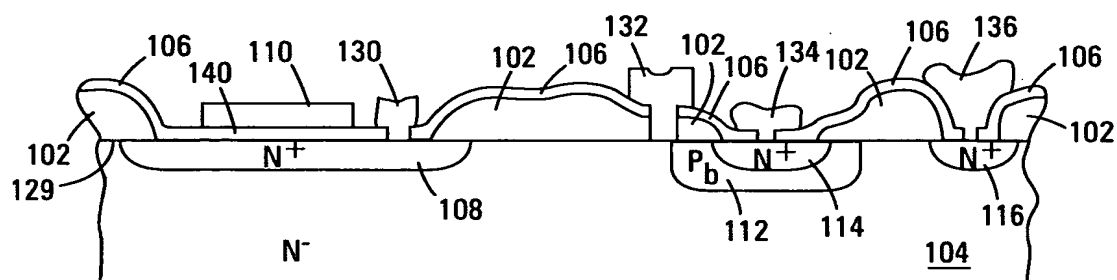
*Fig. 4C*



*Fig. 4D*



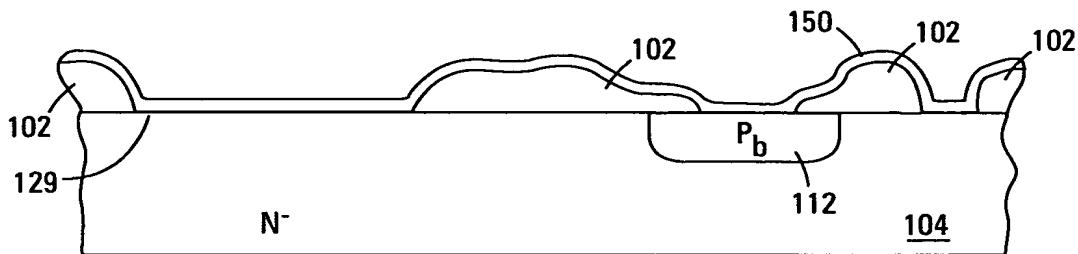
*Fig. 4E*



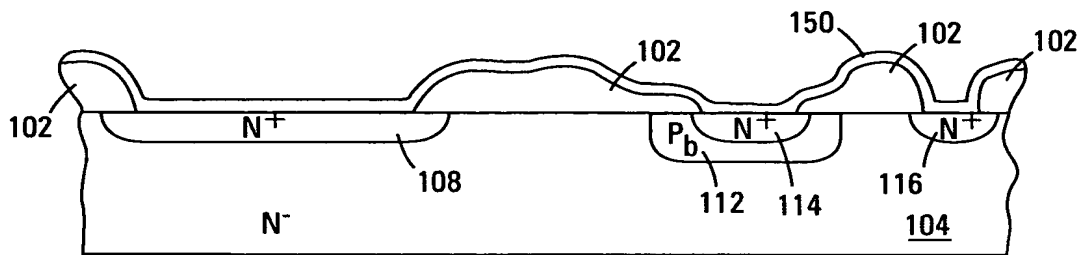
*Fig. 4F*

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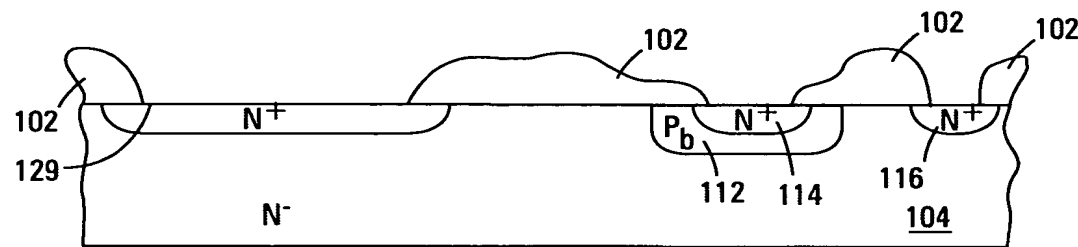
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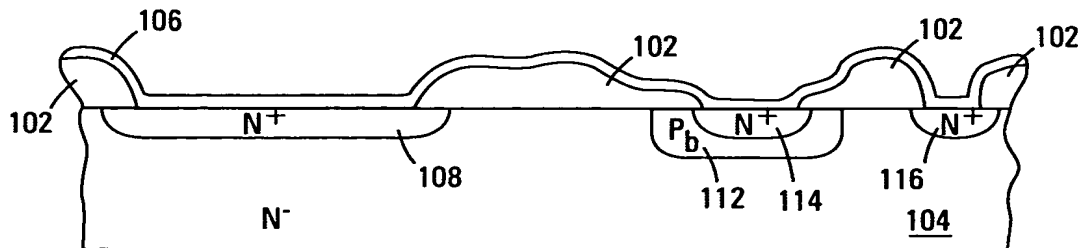
*Fig. 5A*



*Fig. 5B*



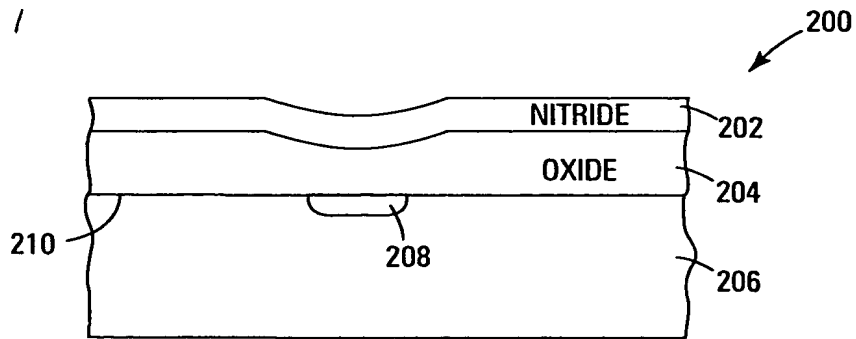
*Fig. 5C*



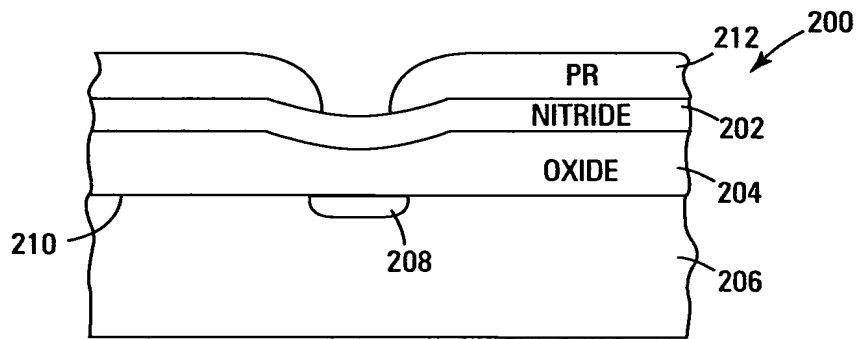
*Fig. 5D*



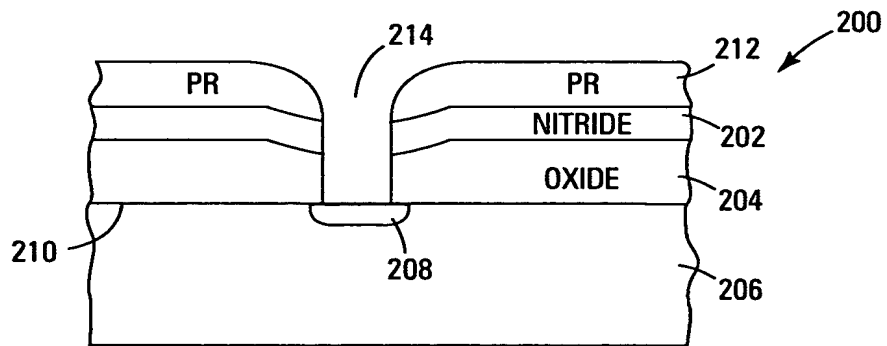
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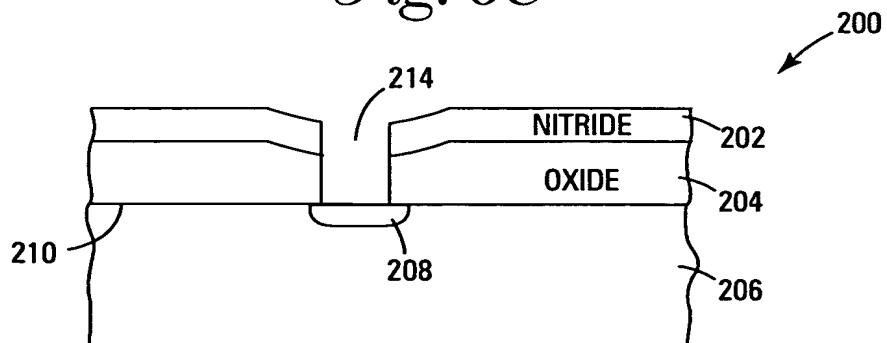
*Fig. 6A*



*Fig. 6B*



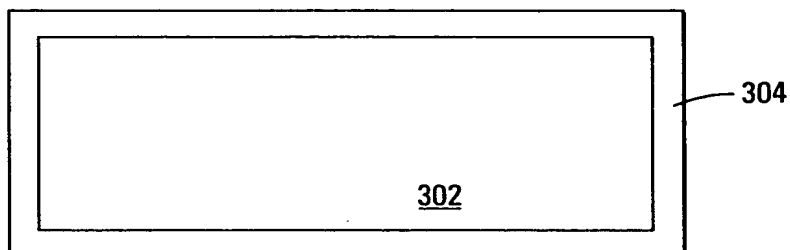
*Fig. 6C*



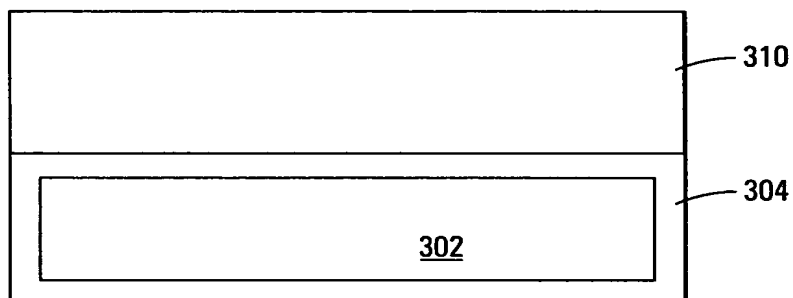
*Fig. 6D*



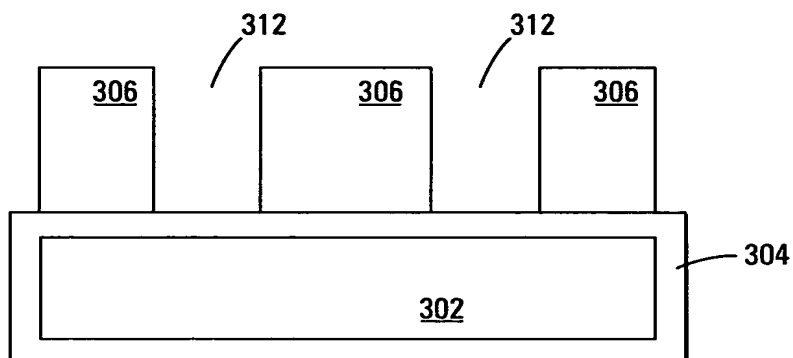
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*Fig. 7A*  
(Prior Art)

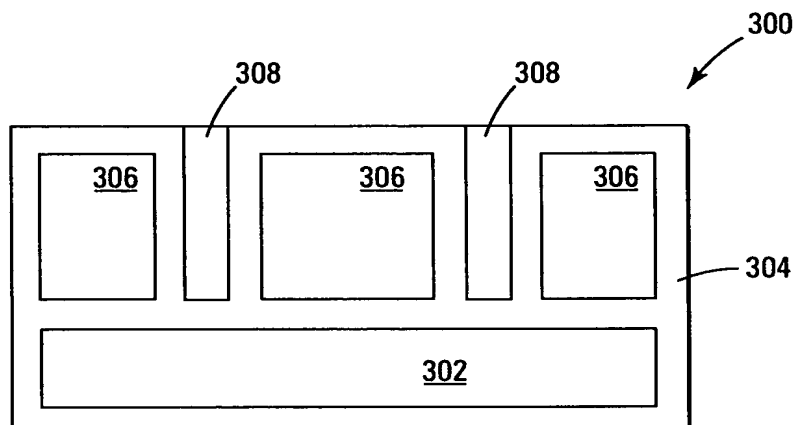


*Fig. 7B*  
(Prior Art)



*Fig. 7C*  
(Prior Art)





*Fig. 7D*  
*(Prior Art)*